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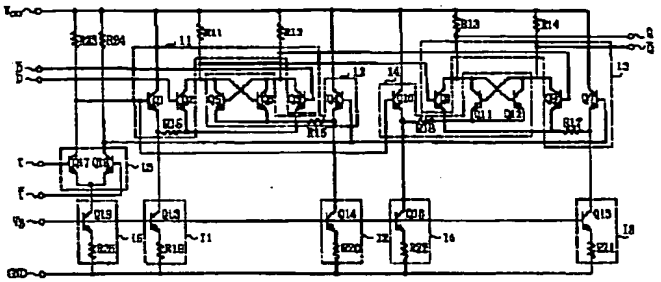
TITLE : LATCH CIRCUIT AND FLIP FLOP CIRCUIT USING THE CIRCUIT



ABSTRACT : PROBLEM TO BE SOLVED: To realize an operation with a low voltage in a latch circuit and a flip flop circuit of the emitter coupled logic system by connecting emitters of transistors TRs, to which a T input signal is inputted, and a TR, to which a D input signal is inputted, through an emitter feedback resistance for switching.

SOLUTION: A clock input T and a signal of the inverted T are inputted to a fifth TR differential pair 15, and a data input signal D and a signal being the inverse of D are inputted to a first differential pair 11. Emitter feedback resistances R15 to R18 for switching of differential pairs consisting of three TRs are inserted in the unbalanced state in first to fourth differential pairs 11 to 14. By this constitution, the number of piled-up stages of TRs connected between a power source V_{CC} and a ground potential GND is two stage because of the stage of TRs Q1 to Q12 constituting differential pairs 11 to 14 and the stage of TRs Q13 to Q16 constituting first to fourth contact current sources 11 to 14, and it is one stage smaller than conventional.